ABSTRACT OF THE DISCLOSURE

In order to correct the duty cycle of a given clock signal to produce a clock signal with a 50% duty cycle, a duty cycle correction circuit includes a delay unit for delaying a first clock signal to output a second clock signal and a clock-signal output unit. The clock-signal output unit includes two transistors which use the first and second clock signals as the inputs of respective gates and an inverter circuit for inverting a signal output from a common drain of the transistors to output a third clock signal. The delay unit delays the first clock signal so that the first clock signal falling appears at a timing at which the duty cycle thereof becomes 50%. The two transistors in the clock-signal output unit output, as the third clock signal, a ground voltage and a source voltage as the signal from the common drain in response to the rising of the first clock signal and the falling of the second clock signal, respectively.